120

05-25-04

AF/2188

ZAGORIN, O'BRIEN & GRAHAM, L.L.P.
7600B N. CAPITAL OF TEXAS HWY, SUITE 350
AUSTIN, TEXAS 78731-1191
INTELLECTUAL PROPERTY ATTORNEYS
512-338-6300 (TEL)
512-338-6301 (FAX)
INTERNET: www.ip-counsel.com

May 24, 2004

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL SHEET

Applicant: Frank P. Helms
Title: MEMORY AND APPARATUS FOR POWERING DOWN THE CPU/MEMORY CONTROLLER COMPLEX WHILE PRESERVING THE SELF REFRESH STATE OF MEMORY IN THE SYSTEM
Application No.: 09/584,301 Filed: May 31, 2000
Atty. Docket No.: 1001-0119 Client Ref. No.: TT3375

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

- ☐ Response to Non-Final Office action(page(s))
- ☐ Petition for Extension of Time (month) (page(s))
- ☐ Information Disclosure Statement (page(s)), including PTO Form 1449 (page(s)), and copies of reference(s)
- ☒ Other: Appelant's Brief (in triplicate) (13 page(s))
- ☐ Other: (page(s))
- ☐ Other: (page(s))
- ☒ Transmittal Letter (2 pages), in duplicate;
- ☒ Return postcard;

The Total Fee has been calculated as shown below:

	Pending Claims	Claims Previously Paid	Extra Claims	Fees
Total Claims	30	– 30 =	0 x $18.00 =	0.00
Independent Claims	7	– 7 =	0 x $86.00 =	0.00
Multiple Dependent Claims (if any) - $290.00 fee				
Additional Claims Fee				$ .00
Fee For Extension Of Time				
Other Fees: (Filing of an Appeal Brief)				330.00
TOTAL FEE DUE:				$ 330.00

- ☐ Applicant is, or has established status as, a small entity.
- ☐ A check is enclosed for the Total Fee shown above.
- ☒ Please charge the Total Fee shown above to Deposit Account 01-0365.
- ☒ The Commissioner is hereby authorized to charge any additional fees under 37 C.F.R. § 1.16 or 1.17 which may be required during the pendency of this application, and to similarly credit any overpayment, to Deposit Account 01-0365.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

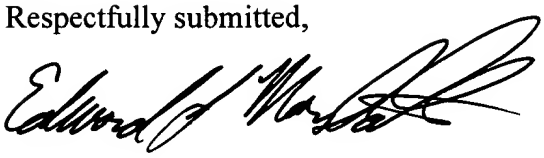
☐ deposited with the US Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

☐ facsimile transmitted to the US Patent and Trademark Office.

_____ _____
Date

EXPRESS MAIL LABEL: EV401039264US

Respectfully submitted,



Edward J. Marshall, Reg. No. 45,395
Attorney for Applicant
(512) 338-6321
(512) 338-6301 (fax)

#10 pay 6-8-04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Frank P. Helms

Title: MEMORY AND APPARATUS FOR POWERING DOWN THE CPU/MEMORY CONTROLLER COMPLEX WHILE PRESERVING THE SELF REFRESH STATE OF MEMORY IN THE SYSTEM

Application No.:	09/584,301	Filed:	May 31, 2000
Examiner:	Thang H. Ho	Group Art Unit:	2188
Atty. Docket No.:	1001-0119	Confirmation No:	3171

May 22, 2004

Mail Stop Appeal Brief - Patents
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313

APPELLANT'S BRIEF (37 C.F.R. § 1.192)

This brief is in furtherance of the Notice of Appeal, filed on March 22, 2004. The fees required under § 1.17(c) are provided in the accompanying Transmittal. The Notice of Appeal was received by the Office on March 22, 2004, thereby setting May 22, 2004 as the date for filing Appellant's Brief. As May 22, 2004 is a Saturday, the time period for filing is extended to Monday May 24, 2004. This brief is being transmitted in triplicate pursuant to 37 C.F.R. § 1.192(a).

REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc., as evidenced by the assignment recorded at Reel 10855/Frame 0076.

RELATED APPEALS AND INTERFERENCES

Appellant has no knowledge of any related appeals or interferences.

STATUS OF CLAIMS

Claims 1-27 and 31-33 are presented herein on appeal. Claims 1, 5, 8, 13-14, 17, 21, 26, and 31 have been amended or added during prosecution. Claims 28-30 and 34 have been cancelled. Claims 2-4, 6-7, 9-12, 15-16, 18-20, 22-25, 27, and 32-33 remain as originally filed.

Most recently, claims 13, 14, and 26 were amended on February 17, 2004, in response to a final Office action, dated December 16, 2003, in which claims 1-33 were finally rejected. The final rejection of Claims 1-27 and 31-33 was maintained in an advisory action dated March 3, 2004 and the claim amendments to claims 13, 14 and 26 were entered. That final rejection is now appealed.

Claims 1-27 and 31-33, now presented herein on appeal, are reproduced in the Appendix attached hereto.

STATUS OF AMENDMENTS

Amendments to Claims 13, 14, and 26 were submitted on February 17, 2004 in a response to a final Office action. The amendments were entered for purposes of Appeal.

SUMMARY OF INVENTION

The presently claimed invention relates to controlling memory systems, and more particularly, to maintaining system memory in a self refresh state during a power savings state in which power is removed from the memory controller.

In one embodiment, a memory control signal is supplied to a memory from a first integrated circuit during an operational state (e.g. a normal run state), and from a different location (e.g. power management logic) during a power savings state. Refer, for example to Fig. 2 of Appellants' specification. During the operational state, clock enable signal CKE 213, supplied by memory controller 206, is used to control memory 204. In a power savings state, however, power to memory controller 206 is removed, and power management logic 217 supplies signal HLDSREF#, which is used in place of CKE 213. Thus, memory 206 receives a

signal on its CKE input from different locations depending on whether the system is operating in a power savings state or an operational state.

Referring to Fig. 5, switch 224 illustrates one method of controlling which circuit (e.g the memory controller 206 or the power management logic 217) will supply a control signal to memory 204. In the illustrated example, SELFREF# is driven low to isolate memory controller 206 from memory 204, thereby allowing HLDSREF# to control memory 204 when memory controller 206 is powered down. Note that the output of the SouthBridge chip, which supplies the signal HLDSREF#, can be held at a high impedance during a normal operation state so that only the CKE signal 213 from memory controller 206 reaches memory 204.

Figs. 8 and 8A illustrate embodiments in which a reset signal is used to select or deselect the CKE signal 713 generated by memory controller 206.

ISSUES

The issues on appeal are whether Appellant's claims 1-27 and 31-33 are anticipated by U.S. Patent No. 6,212,599 (Baweja) under 35 USC § 102(e), or unpatentable over Baweja under 35 USC § 103(a).

GROUPING OF CLAIMS

Group 1: 1-7

Group 2: 14, 19, and 20

Group 3: 10, 11, 13, 18, 21, and 23-25

Group 4 26-27, and 31-33

Group 5: 8-9, 12 15-17, and 22

ARGUMENTS

Baweja Does Not Teach or Suggest All Elements of the Appellant's Claims.

Group 1

All claims of the first group have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,212,599 (Baweja). For purposes of this discussion, claim 1 of Group 1 will be addressed. Appellant respectfully maintains that Baweja does not teach or suggest supplying a memory control signal from a first integrated circuit according to an operational state and from another location in the self refresh state, as required generally by claim 1.

Notwithstanding the Office's assertion to the contrary, Appellant submits that the clock enable signal CKE 330 (Baweja, Fig. 3), cited by the Office as meeting the claimed limitations of Appellant's claim 1, is not supplied from a first integrated circuit according to an operational state and from another location in the self refresh state. Clock enable signal CKE 330 may be generated based on signals SDCKE 240 and SCKE (Baweja, Fig. 3), but that does not change the fact that Baweja's signal CKE 330 is supplied from the same location during both operational states and during a self refresh state. While it may be true that the value of clock enable signal CKE 330 is different during operational and self refresh states, the signal itself is not supplied from different locations.

The Office takes the position that the CKE signal is supplied by suspend memory controller 220 during the sleep mode and by the first memory controller 210 during normal operation (see advisory action dated March 3, 2004). In fact, suspend controller 220 and first memory controller 210 are both a part of memory controller 200 (Baweja, Fig. 2; col. 4, ll. 14-19), which provides the CKE signal at all times.

For at least these reasons, the cited references fail to teach or suggest the claimed invention. The Office's rejection of claim 1, and all claims of Group 1, should therefore, be reversed.

Group 2

All claims of the second group have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,212,599 (Baweja). For purposes of this discussion, Claim 14 of Group 2 will be addressed. Appellant respectfully maintains that Baweja does not teach or

suggest a memory control circuit coupled to system memory to provide a control signal during operational state, and a second circuit, independent of the memory control circuit, coupled to cause the memory control signal to be at the first value during a power saving state, as required generally by claim 14.

The system disclosed in Baweja includes a first memory controller 210 and a suspend memory controller 220, which together form memory system controller 200. First memory controller 210 and suspend memory controller 220, however, are not independent of each other. During normal operation, the suspend memory controller 220 acts as part of the memory system controller 200 (Baweja, col. 4, ll. 32-34). Thus, the value of clock enable signal CKE 330 (Baweja, Fig. 3) or CKE 260 (Baweja, Fig. 2) is not determined by a second circuit, independent of the memory control circuit. In fact, memory system controller 200 determines the value of the clock enable signal at all times, based on the signals SDCKE 240 and SCKE (Baweja, Fig. 3).

For at least these reasons, the cited references fail to teach or suggest the claimed invention. The Office's rejection of claim 14, and all claims of Group 2, should therefore, be reversed.

Group 3

All claims of the third group have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,212, 599 (Baweja). For purposes of this discussion, Claim 21 of Group 3 will be addressed. Appellant respectfully maintains that Baweja does not teach or suggest means for holding an output terminal at a high impedance during the operational state, and providing a first logic level through the output terminal during a power saving state, as required generally by claim 21 and shown, e.g. in Fig. 2.

The system disclosed in Baweja uses AND gate 320 to supply a clock enable signal CKE 330 based on signals SDCKE 240 and SCKE during both operational and power saving states. If the output of AND gate 320 were to be held at a high impedance during the operational state, the clock enable signal CKE 330 would not reach the memory during the operational state, and the system of Baweja would be inoperable.

For at least these reasons, the cited references fail to teach or suggest the claimed invention. The Office's rejection of claim 21, and all claims of Group 3, should therefore, be reversed.

Group 4

All claims of the fourth group have been rejected either under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,212, 599 (Baweja), or under 35 U.S.C. §103(a) as being unpatentable over Baweja. For purposes of this discussion, Claim 26 of Group 4 will be addressed. Appellant respectfully maintains that Baweja does not teach or suggest that an asserted reset signal holds a memory control signal at a value to keep the memory in a self-refresh state, as required generally by claim 26.

The system disclosed in Baweja uses a clock enable signal CKE supplied by AND gate 320 to maintain a memory in a self refresh state (Baweja, col. 5, ll. 13-14, "The self-refresh mode is maintained by holding CKE low"). The value of CKE 330 is determined by the state of signals SDCKE 240 and SCKE during both operational and power saving states. There is no teaching or suggestion in Baweja that an asserted reset signal holds CKE 330 at a particular value to keep the memory in a self-refresh state.

For at least these reasons, the cited references fail to teach or suggest the claimed invention. The Office's rejection of claim 26, and all claims of Group 4, should therefore, be reversed.

Group 5

All claims of the fifth group have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,212, 599 (Baweja). For purposes of this discussion, Claim 8 of Group 5 will be addressed. Appellant respectfully maintains that Baweja does not teach or suggest isolating a first integrated circuit, which supplies a memory control signal to a memory during an operational state, from the memory during a power saving state, as required generally by claim 8.

Figs. 2 and 3 of Baweja illustrate first memory controller 210 and suspend memory controller 220, which together form memory system controller 200. The memory system controller 200 controls the clock enable signal CKE 260 (Fig. 2) or CKE 330 (Fig. 3) during both operational and power saving states. The memory system controller 200 is, therefore, not a first integrated circuit isolated from the memory during the power saving state. If memory system controller 200 were to be isolated from the memory during the power saving state, the memory would not receive memory clock enable signal CKE 260 or CKE 330 during the power saving state.

For at least these reasons, the cited references fail to teach or suggest the claimed invention. The Office's rejection of claim 8, and all claims of Group 5, should therefore, be reversed.

CONCLUSION

For at least the foregoing reasons, Appellant's claimed invention is not anticipated by, nor obvious over, the cited prior art. Accordingly, this Board is respectfully requested to reverse the rejection of claims 1-27 and 33, and direct this application to be issued.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

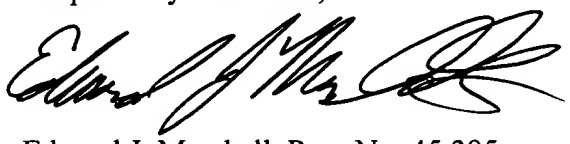
☐ deposited with the US Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

☐ facsimile transmitted to the US Patent and Trademark Office.

_____ _____
Date

EXPRESS MAIL LABEL: EV401039264US

Respectfully submitted,



Edward J. Marshall, Reg. No. 45,395
Attorney for Applicant(s)
(512) 338-6321
(512) 338-6301 (fax)

APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

1. A method for controlling a self refresh state of memory in a computer system, comprising:

supplying at least one memory control signal to the memory from a first integrated circuit in the computer system according to an operational state; and

supplying the memory control signal from another location in the computer system when the computer system is in a power savings state to maintain memory in the self refresh state.

2. The method as recited in claim 1 wherein the first integrated circuit is completely powered off during the power savings state.

3. The method as recited in claim 1 wherein the power savings state is a suspend to RAM state.

4. The method as recited in 1 wherein the memory control signal is a clock enable signal.

5. The method as recited in 1 wherein the memory control signal is a reset signal.

6. The method as recited in claim 4 wherein the clock enable signal is low while the memory is maintained in the self refresh state.

7. The method as recited in claim 1 wherein the memory control signal is held at a first value to keep the memory in the self refresh state.

8. A method for controlling a self refresh state of memory in a computer system, comprising:

controlling at least one memory control signal being supplied to the memory from a first integrated circuit in the computer system according to an operational state;

controlling the memory control signal from another location in the computer system when the computer system is in a power savings state to maintain memory in the self refresh state; and

isolating the first integrated circuit from the memory during the power savings state.

9. The method as recited in claim 8 wherein isolating further includes disabling a switch coupling the memory control signal from the first integrated circuit to the memory by driving a switch enable signal to a first predetermined value to turn off the switch, the switch enable signal being driven from the other location.

10. The method as recited in claim 9 further comprising driving a signal line which is coupled to the switch and is coupled to the memory control signal input to the memory to a predetermined logical level from the other location, during the power savings state to control the memory control signal and wherein the signal line is driven at a high impedance by the other location during the operational state.

11. The method as recited in claim 10 wherein the switch enable signal is at a second predetermined value to turn on the switch during the operational state.

12. The method as recited in claim 9 wherein the other location drives the signal line coupled to the switch and coupled to the memory control signal input to the memory before the switch enable signal is driven to the first predetermined value to turn off the switch and wherein the switch enable signal is driven to the second predetermined value to turn on the switch before the other location drives the signal at high impedance.

13. The method as recited in claim 1 wherein the first integrated circuit drives the memory control signal at at least a first logical level during the operational state and the other location drives the memory control signal at a high impedance level during the operational state and wherein the first integrated circuit is powered off during the power savings state and the other location drives the memory control signal at a second logical level during the power savings state, to keep the memory in the self refresh state.

14. A computer system comprising:

a system memory capable of operating in a self refresh state, the system memory coupled to receive at least one memory control signal required to be held at a first value during the self refresh state;

a memory control circuit coupled to the system memory to provide at least one memory control signal during an operational state; and

a second circuit independent of the memory control circuit, coupled to cause the memory control signal to be at the first value during a power savings state.

15. The computer system as recited in claim 14 further comprising an isolation circuit coupled between the memory control circuit and the memory, the isolation circuit being coupled to receive the memory control signal from the memory control circuit and to selectably provide the memory control signal from the memory control circuit to the memory.

16. The computer system as recited in claim 15 wherein the second circuit is coupled to provide a high impedance on an output terminal, during an operational state of the computer system, the output terminal being coupled to the isolation circuit and the memory to provide the memory control signal, and wherein the second circuit is coupled to drive the output terminal and thereby the memory control signal to a low voltage level during the power savings state.

17. The computer system as recited in claim 15 wherein the second circuit is coupled to provide an isolation control signal to the isolation circuit during the power savings state to isolate the memory control signal provided from the memory control circuit from the memory, during the power savings state.

18. The computer system as recited in claim 14 wherein the second circuit is coupled to provide a high impedance on an output terminal that is coupled to the memory control signal during an operational state of the computer system and wherein the second circuit provides a logical level on the output terminal to drive the memory control signal to the first value during the power savings state.

19. The computer system as recited in claim 14 wherein the power savings state is a suspend to RAM state wherein system context is stored in the system memory during the suspend to RAM state.

20. The computer system as recited in claim 14 wherein the memory control circuit is on an integrated circuit having multiple power planes and all power planes are powered down during the power savings state.

21. A computer system comprising:

first means for controlling system memory during an operational state; and

second means for controlling the system memory during a power savings state to maintain the system memory in a self refresh state when the first means is completely powered off, the second means including means for holding an output terminal at a high impedance during the operational state and means for providing a first logic level through the output terminal during the power savings state.

22. The computer system as recited in claim 21 further comprising isolation means to isolate the first means from the system memory during the power savings state.

23. The computer system as recited in claim 21 wherein the first and second means are disposed on one integrated circuit.

24. An integrated circuit of a computer system comprising:

a first output terminal for coupling to a memory control signal that is held at a first logic level to keep a memory in a self refresh state, the integrated circuit responsive to a first operational state of the computer system to place the output terminal at a high impedance level and responsive to a power savings state in the computer system to supply the first logic level on the output terminal.

25. The integrated circuit as recited in claim 24 further comprising a second output terminal for coupling to a switch, the integrated circuit responsive to the first operational state of the computer system to place the second output terminal at a logic level causing the switch to

pass through a memory control signal coupled to the switch and responsive to the power savings state to supply a different logic level at the output terminal, the second logic level causing the switch to not pass through the memory control signal.

26. A method for controlling a self refresh state of a memory in a computer system, comprising:

controlling at least one memory control signal being supplied to the memory from a first region in an integrated circuit in the computer system during an operational state;

controlling the at least one memory control signal from another location in the integrated circuit during a power savings state in which the first region is not powered, to maintain memory in the self refresh state;

wherein the memory control signal is held at a first value to keep the memory in the self refresh state; and

wherein an asserted reset signal holds the memory control signal at the first value in the first integrated circuit during the power savings state.

27. The method as recited in claim 26 wherein the power savings state is a an S3 suspend to RAM state.

28. (Canceled)

29. (Canceled)

30. (Canceled)

31. An apparatus comprising:

a memory control circuit coupled to control at least one memory control signal during an operational state; and

a second circuit coupled to cause the memory control signal to be at a logic level to maintain a memory in a self refresh state, the second circuit being operational during a power savings state in which power to the memory control circuit is turned off, wherein a reset signal coupled to the second circuit, when asserted,

causes the second circuit to keep the memory control signal at the logic level to maintain the memory in a self refresh state.

32. The apparatus as recited in claim 31 wherein the memory control circuit and the second circuit are disposed on one integrated circuit.

33. The apparatus as recited in claim 32 wherein the integrated circuit includes the memory control circuit and a central processing circuit (CPU).

34. (Canceled)